WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a memory capacitor that is formed on an insulating layer over a semiconductor substrate and includes a lower electrode, an upper electrode and a capacitor insulating film disposed between said lower electrode and said upper electrode;

a capacitor insulating film extension and an upper electrode extension extending respectively from said capacitor insulating film and said upper electrode of said memory capacitor;

a dummy conducting member including a portion below said upper electrode extension and said capacitor insulating film extension;

a conducting member in contact with side faces of said upper electrode extension and said capacitor insulating film extension and connected to said dummy conducting member; and

an upper interconnect electrically connected to said dummy conducting member.

2. The semiconductor memory of Claim 1,

wherein said conducting member covers the side faces of said upper electrode extension and said capacitor insulating film extension to surround the entire circumference of films that include said upper electrode and extension thereof, and said capacitor insulating film and extension thereof, respectively.

3. The semiconductor memory of Claim 1 or 2,

wherein said dummy conducting member includes a dummy lower electrode, said dummy lower electrode and said lower electrode being made from an identical conductor film, and

said conducting member electrically connects said upper electrode extension to said dummy lower electrode.

4. The semiconductor memory of Claim 1 or 2,

wherein said conducting member entirely covers said upper electrode and said upper electrode extension.

5. The semiconductor memory of Claim 3, further comprising:

a bit line formed below said memory capacitor with said insulating layer sandwiched therebetween; and

a local interconnect, said local interconnect and said bit line being made from an identical conductor film,

wherein said dummy conducting member includes a conducting plug for connecting said dummy lower electrode and said local interconnect to each other through said insulating layer.

6. The semiconductor memory of Claim 3, further comprising:

an isolation insulating film provided on said semiconductor substrate below said insulating layer;

a memory cell transistor that is provided on said semiconductor substrate in a region surrounded with said isolation insulating film and includes a gate electrode and impurity diffusion layers formed in said semiconductor substrate on both sides of said gate electrode;

a local interconnect formed on said isolation insulating film, said local interconnect and said gate electrode being made from an identical conductor film; and

a conducting plug connected to said local interconnect through said interlayer insulating film.

7. The semiconductor memory of Claim 3, further comprising:

a memory cell transistor that is provided on said semiconductor substrate and includes a gate electrode and impurity diffusion layers formed in said semiconductor

substrate on both sides of said gate electrode;

a local interconnect made from another impurity diffusion layer spaced from said impurity diffusion layers in said semiconductor substrate; and

a conducting plug connected to said local interconnect through said insulating layer.

8. The semiconductor memory of Claim 1 or 2,

wherein said dummy conducting member is provided in a region surrounded, on a side face thereof, with at least said insulating layer, and

said conducting member is in contact with said upper electrode extension and said dummy conducting member.

9. The semiconductor memory of Claim 8,

wherein said dummy conducting member is a local interconnect, and

said upper interconnect is in contact with said local interconnect.

10. The semiconductor memory of Claim 8,

wherein said dummy conducting member is a dummy plug, and

said conducting member is in contact with at least a part of a top face of said dummy plug.

11. The semiconductor memory of Claim 8,

wherein said conducting member is a conducting sidewall that is provided over side faces of said upper electrode extension and said capacitor insulating film extension and is in contact with at least a part of a top face of said dummy conducting member.

12. The semiconductor memory of Claim 1 or 2,

wherein said capacitor insulating film is a high- κ film or a ferroelectric film.

13. A method for fabricating a semiconductor memory containing a memory capacitor including a lower electrode, an upper electrode and a capacitor insulating film

disposed between said lower electrode and said upper electrode; a dummy conducting member electrically connected to said upper electrode; and an upper interconnect electrically connected to said dummy conducting member, comprising the steps of:

(a) forming said lower electrode by forming a first conductor film over an insulating layer on a semiconductor substrate and patterning said first conductor film;

(b) forming a dielectric film covering said lower electrode;

(c) forming a second conductor film covering said dielectric film;

(d) forming, on said second conductor film, an etching mask covering a part of said lower electrode;

(e) patterning said second conductor film and said dielectric film, whereby forming said capacitor insulating film and a capacitor insulating film extension from said dielectric film and said upper electrode and an upper electrode extension from said second conductor film; and

(f) depositing a third conductor film on said substrate after the step (e) and patterning said third conductor film, whereby forming a conducting member in contact with side faces of said upper electrode extension and said capacitor insulating film extension and electrically connected to said dummy conducting member.

14. The method for fabricating a semiconductor memory of Claim 13,

wherein said lower electrode and a dummy film spaced away from said lower electrode are formed by patterning said first conductor film in the step (a),

a dummy lower electrode is formed as at least a part of said dummy conducting member by patterning said dummy film in any step between the step (b) and the step (e), and

said conducting member formed in the step (f) is in contact with side faces of said upper electrode extension, said capacitor insulating film extension and said dummy lower

electrode and covers at least a part of a portion above said upper electrode extension.

15. The method for fabricating a semiconductor memory of Claim 13, further comprising, before the step (a), a step of forming at least a part of said dummy conducting member in a region surrounded, on a side face thereof, with said insulating layer,

wherein said conducting member formed in the step (f) is in contact with at least a part of a top face of said dummy conducting member.

16. The method for fabricating a semiconductor memory of Claim 15,

wherein said conducting member formed in the step (f) is a conductor film that is in contact with the side faces of said upper electrode extension and said capacitor insulating film extension and covers at least a part of a portion above said upper electrode extension.

17. The method for fabricating a semiconductor memory of Claim 15,

wherein said conducting member formed in the step (f) is a conducting sidewall in contact with the side faces of said upper electrode extension and said capacitor insulating film extension.

18. The method for fabricating a semiconductor memory of any of Claims 13 through 17,

wherein said dielectric film is a high- κ film or a ferroelectric film.